33. (Amended) A trench-isolated transistor comprising:

first and second isolation trenches each disposed on a respective side of a portion of silicon, the first and second isolation trenches each comprising:

a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the silicon at a first angle;

a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at a second angle with respect to the surface that is greater than the first angle; and

a dielectric material filling the first and second isolation trench portions, the transistor further comprising:

a gate extending across the silicon portion from the first isolation trench to the second isolation trench; and

source and drain regions extending between the first and second isolation trench portions and across the silicon portion, the source region being disposed adjacent one side of the gate and the drain region being disposed adjacent another side of the gate that is opposed to the one side.

34. (Amended) The trench-isolated transistor of claim 33, wherein at least some of the first sidewall forms a substantially straight linear segment.

35. The trench-isolated transistor of claim 33, wherein the second angle is between eighty and ninety degrees.

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36. The trench-isolated transistor of claim 33, wherein the first angle is in a range of from about thirty degrees to about seventy degrees and the second angle is more than eighty degrees.

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37. (Amended) The trench-isolated transistor of claim 33, wherein the first depth is between five and fifty percent of a total trench depth.

38. The trench-isolated transistor of claim 33, wherein the dielectric material filling the first and second isolation trench portions has a planar surface.

NE

39. The trench-isolated transistor of claim 33, wherein the first angle is in a range of from about thirty degrees to about seventy degrees.

40. The trench-isolated transistor of claim 39, wherein the second angle is in a range of from eighty to ninety degrees.

41. The trench-isolated transistor of claim 33, wherein the transistor is formed as a part of a memory integrated circuit.

42. (Amended) A trench isolation structure formed in a semiconductor comprising:

a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle;

a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at a second angle with respect to the surface that is greater than the first angle; and

a dielectric material filling the first and second isolation trench portions.

43. (Amended) The trench isolation structure of claim 42, wherein at least some of the first isolation trench portion forms a substantially straight linear segment.

44. The trench isolation structure of claim 42, wherein the first angle is in a range of from about thirty degrees to about seventy degrees and the second angle is more than eighty degrees.

45. The trench isolation structure of claim 42, wherein the first angle is in a range of from about thirty degrees to about seventy degrees.

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46. (Amended) The trench isolation structure of claim 42, wherein the first depth is between five and fifty percent of a total trench depth.

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47. The trench isolation structure of claim 42, wherein the trench isolation structure is formed in a memory integrated circuit.

48. (Amended) A memory cell including:

a capacitor;

a trench-isolated transistor having a gate, a drain and a source, the source being coupled to one terminal of the capacitor, the trench-isolated transistor including:

first and second isolation trenches each disposed on a respective side of a portion of silicon, the first and second isolation trenches each comprising:

a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the silicon at a first angle;

a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at a second angle with respect to the surface that is greater than the first angle; and

a dielectric material filling the first and second isolation trench portions;

the transistor further comprising:

a gate extending across the silicon portion from the first isolation trench to the second isolation trench; and

source and drain regions extending between the first and second isolation trench portions and across the silicon portion, the source region

being disposed adjacent one side of the gate and the drain region being disposed adjacent another side of the gate that is opposed to the one side; the memory cell further including:

a bitline coupled to the drain; and

a wordline coupled to the gate.

49. The memory cell of claim 48, wherein the gate comprises polysilicon.

50. (Amended) The memory cell of claim 48, wherein at least some of the first sidewall forms a substantially straight linear segment.

51. The memory cell of claim 48, wherein the first angle is in a range of from about thirty degrees to about seventy degrees and the second angle is more than eighty degrees.

52. The memory cell of claim 48, wherein the first angle is in a range of from about thirty degrees to about seventy degrees.

53. (Amended) The memory cell of claim 48, wherein the first depth is between five and fifty percent of a total trench depth.

54. The memory cell of claim 48, wherein the memory cell is included within a DRAM integrated circuit.

55. (Amended) A DRAM comprising:

address decoding circuitry;

a group of bitlines coupled to the address decoding circuitry and extending in a first direction;

a group of wordlines coupled to the address decoding circuitry and extending in a second direction, each wordline in the group of wordlines intersecting each of the bitlines in the group of bitlines once at an intersection;

a plurality of memory cells each disposed at one of the intersections, each memory cell comprising:

a capacitor;

a trench-isolated transistor having a gate, a drain and a source, the source being coupled to one terminal of the capacitor, the trench-isolated transistor including:

first and second isolation trenches each disposed on a respective side of a portion of silicon, the first and second isolation trenches each comprising:

a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the silicon at a first angle;

a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second

sidewall intersecting the first sidewall at a second angle with respect to the surface that is greater than the first angle; and

a dielectric material filling the first and second isolation trench portions;

the transistor further comprising:

a gate extending across the silicon portion from the first isolation trench to the second isolation trench; and

source and drain regions extending between the first and second isolation trench portions and across the silicon portion, the source region being disposed adjacent one side of the gate and the drain region being disposed adjacent another side of the gate that is opposed to the one side;

each memory cell further including:

one bitline of the group of bitlines coupled to the drain; and

one wordline of the group of wordlines coupled to the gate.

56. (Amended) The DRAM of claim 55, wherein at least some of the first sidewall forms a substantially straight linear segment.

57. The DRAM of claim 55, wherein the gate comprises polysilicon.

58. The DRAM of claim 55, wherein the first angle is in a range of from about thirty degrees to about seventy degrees and the second angle is more than eighty degrees.

59. The DRAM of claim 55, wherein the first angle is in a range of from about thirty degrees to about seventy degrees.

60. (Amended) The DRAM of claim 55, wherein the first depth is between five and fifty percent of a total trench depth.

61. The DRAM of claim 55, wherein the dielectric material filling the first and second isolation trench portions includes a planar outer surface.

New Claims

All Sub B7

62. A memory cell including:

a capacitor;

a trench-isolated transistor having a gate, a drain and a source, the source being coupled to one terminal of the capacitor, the trench-isolated transistor including:

an isolation trench disposed on a respective side of a portion of silicon, the isolation trench comprising:

a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the silicon at a first angle;

a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at a second angle with respect to the surface that is greater than the first angle; and

a dielectric material filling the isolation trench portions;

the transistor further comprising:

a gate extending across the silicon portion from the first isolation trench; and

source and drain regions extending from the isolation trench across the silicon portion, the source region being disposed adjacent one side of the gate and the drain region being disposed adjacent another side of the gate that is opposed to the one side;

the memory cell further including:

a bitline coupled to the drain; and

a wordline coupled to the gate.

63. The memory cell of claim 62, wherein the gate comprises polysilicon.

64. The memory cell of claim 62, wherein at least some of the first sidewall forms a substantially straight linear segment.

65. The memory cell of claim 62, wherein the first angle is in a range of from about thirty degrees to about seventy degrees and the second angle is more than eighty degrees.

66. The memory cell of claim 62, wherein the first angle is in a range of from about thirty degrees to about seventy degrees.

67. The memory cell of claim 62, wherein the first depth is between five and fifty percent of a total trench depth.

68. The memory cell of claim 62, wherein the memory cell is included within a DRAM integrated circuit.

69. The memory cell of claim 62, wherein the isolation trench comprises a first isolation trench, the memory cell further comprising a second isolation trench, the first and second isolation trenches each disposed on a respective side of the portion of silicon, the second isolation trench comprising:

a third isolation trench portion having the first depth and having a third sidewall intersecting the surface at the first angle;

a fourth isolation trench portion within and extending below the third isolation trench portion, the fourth isolation trench portion having the second depth and including a fourth sidewall intersecting the third sidewall at the second angle; and wherein:

the dielectric material fills the first and second isolation trench portions;

the gate extends across the silicon portion from the first isolation trench to the second isolation trench; and

the source and drain regions extend between the first and second isolation trench portions and across the silicon portion, the source region being disposed adjacent one side of the gate and the drain region being disposed adjacent another side of the gate that is opposed to the one side.